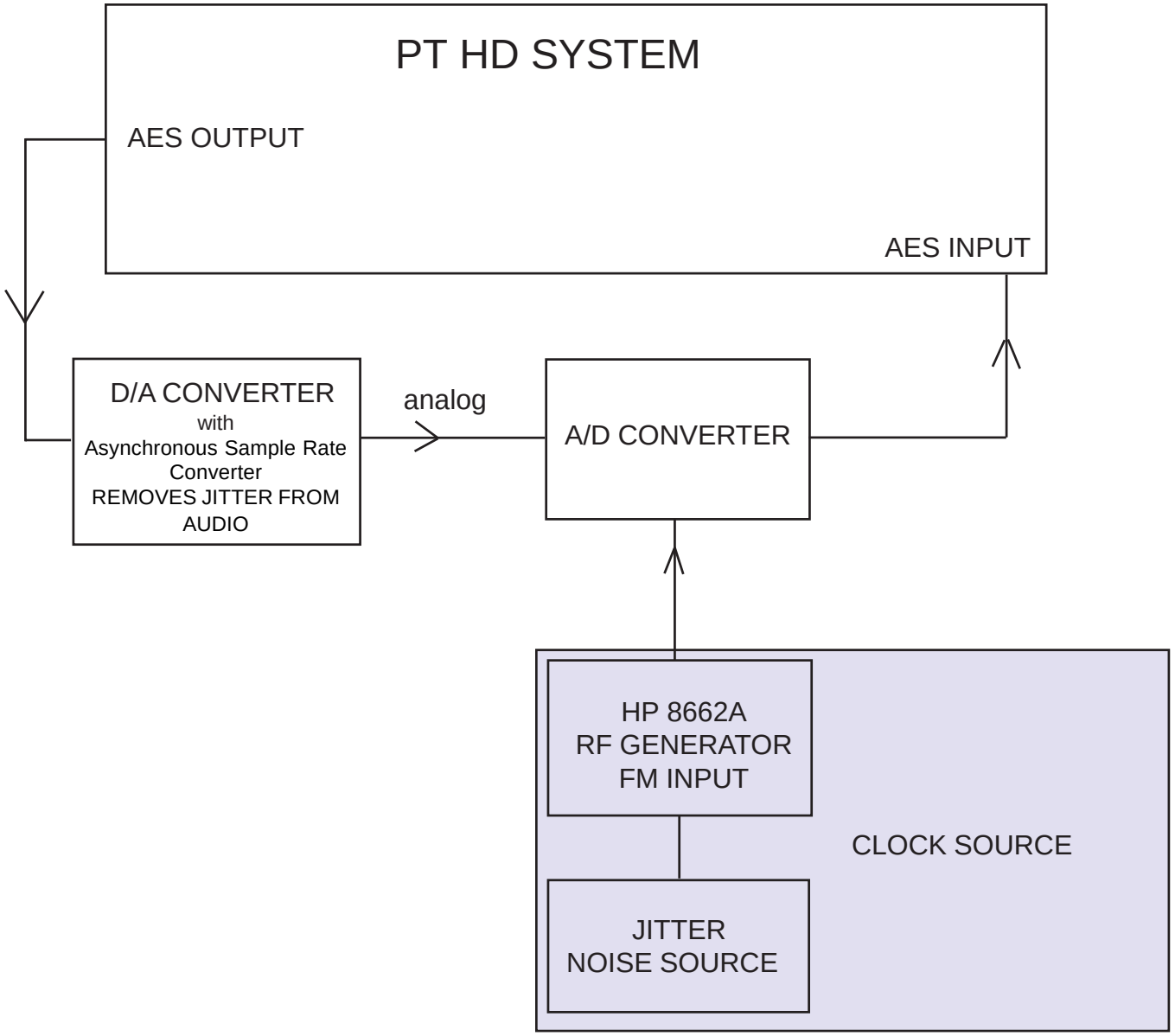
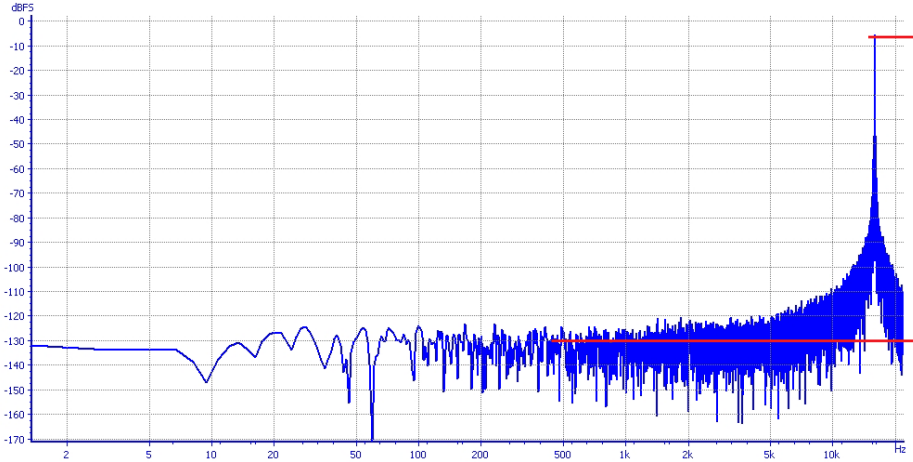
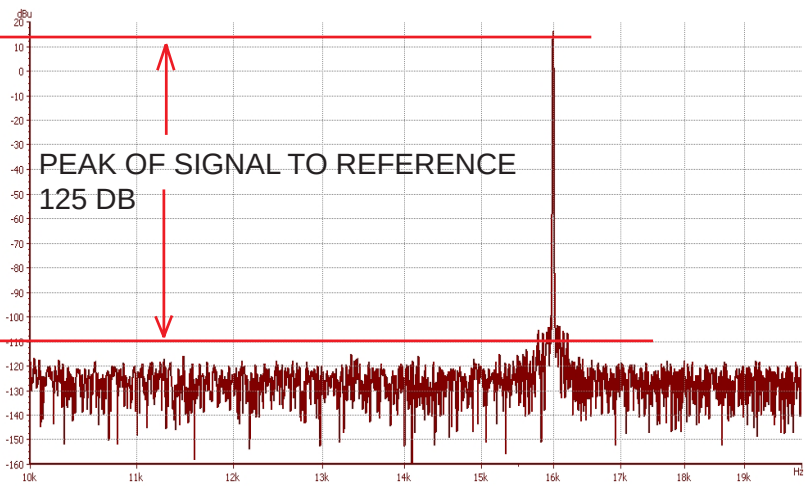


By using this set up the files will line up and phase cancel



16KHz sine wave output from PT with very high system jitter



D/A analog output showing the reduction in jitter due to the Asynchronous Sample Rate Converter. The frequency axis is magnified to show detail. About half of the close in noise in this measurement is due to system imperfections not the ASRC

This shows the reduction in jitter due to the Asynchronous Sample Rate Converter.

Jitter measurements were attempted using a Tektronix TDS7704B with the TDSJIT3 v2 Jitter Analysis Application. They did not work. The one good jitter measurement is at the clock input of the A/D using the Stanford SR1. PT was synchronized to the AES input. The jitter levels are modified by the PLL in the AES receiver of the interface, so the recorded jitter level and spectrum unknown. Being the goal of this is to learn what jitter sounds like and provide education, the actual jitter levels do not matter for the intended purpose.